The Open University of Sri Lanka
Faculty of Engineering Technology

Study Programme	:	Bachelor of Technology Honours in Engineering
Name of the Examination	:	Final Examination
Course Code and Title	:	**MEX3272 – Applied electronics**
Academic Year	:	2016/17
Date	:	17th November 2017
Time	:	0930hr-1230hr
Duration	:	3 hours

General instructions

1. Read the instruction carefully before answering the questions.
2. This question paper has eight questions.
3. Answer **five** questions only.

Q1.

(a) Find the mesh currents (I_1,I_2) in the circuit shown in Figure Q1-a. [04 marks]

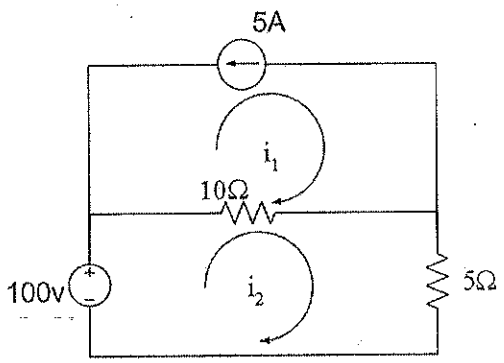


Figure Q1-a

(b) Determine Thévenin and Norton equivalent circuits of the circuit illustrated in Figure Q1-b. [08 marks]

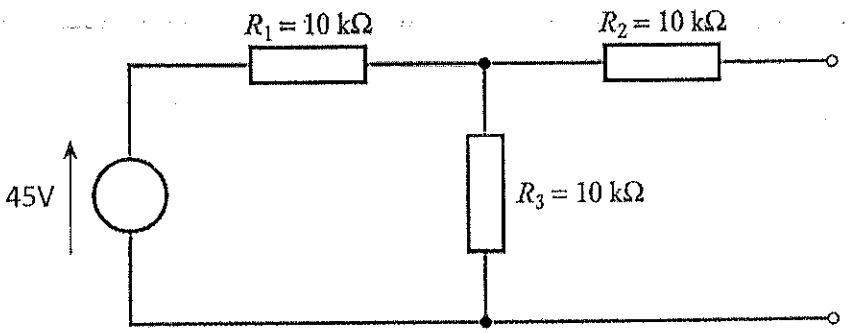


Figure Q1-b

(c) Determine the current I_1 of the circuit shown in Figure Q1-c using nodal analysis.

[04 marks]

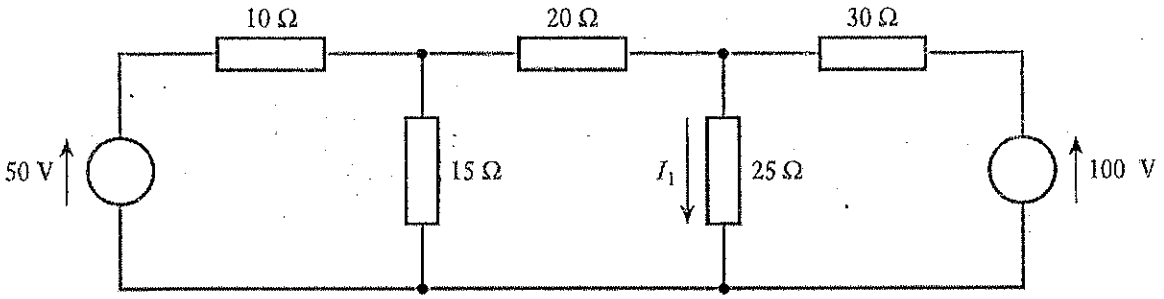


Figure Q1-c

(d) A Wheatstone bridge is used by a student to study how the resistance of a thermistor is affected by its temperature. The thermistor is placed in water at a temperature of 25°C and the resistance of the variable resistor R is adjusted to 450Ω to balance the bridge. Calculate the resistance of the thermistor at that temperature. [04 marks]

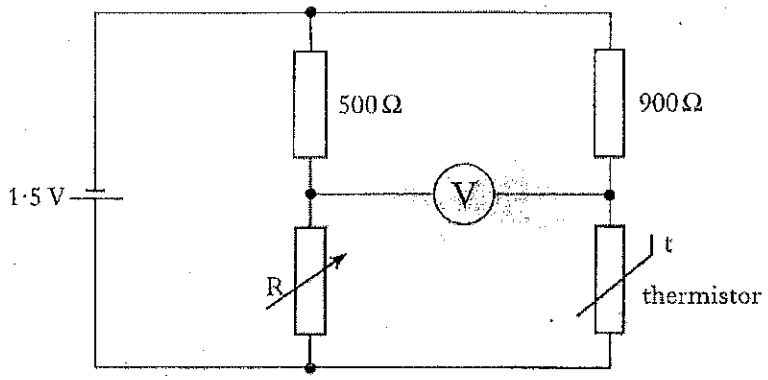


Figure Q1-d

Q2.

(a) i. Sketch the characteristic curves of ideal and real diodes.

ii. Indicate forward current, leakage current and breakdown voltage on the characteristic curve of real diode and explain the characteristics of the diode briefly.

[08 marks]

(b) A zener diode is used in the signal clamping circuit shown in the Figure Q2-b. Sketch the output waveform Vo, if the source is 10V and zener voltage of the diode is 5V.

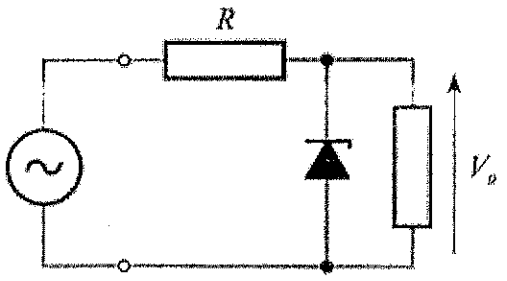


Figure Q2-b [06 marks]

(c) A double diode clipper circuit shown in Figure Q2-c can be used to limit the peaks of both half cycles of the 10V AC input signal. Sketch the output signal.

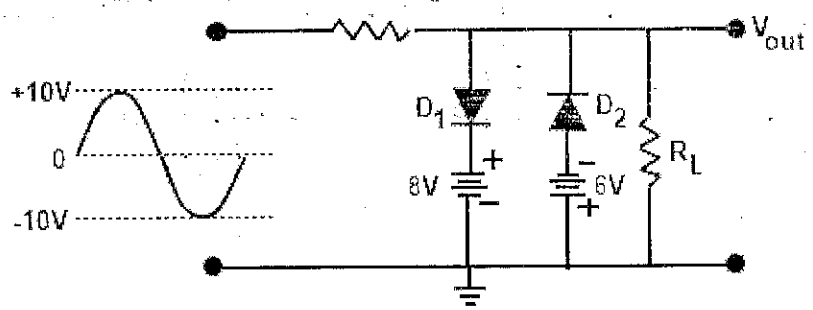


Figure Q2-c

[06 marks]

Q3.

(a) Determine followings of the AC-coupled amplifier shown in the figure Q3-a. (g_m =2 mS) [12 marks]

i. the input resistance,
ii. the output resistance,
iii. the small-signal voltage gain
iv. low-frequency cut-off

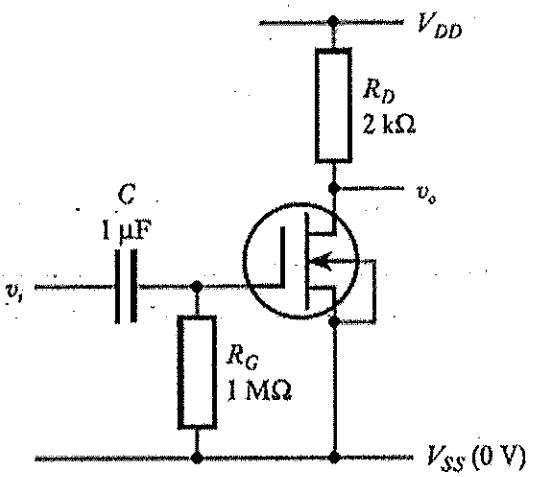


Figure Q3-a

(b) Briefly explain any two applications of FET. [08 marks]

Q4.

(a) Determine V_B, V_E, I_E, I_C and Vo of the BJT amplifier circuit shown in figure Q4-a. [12 marks]

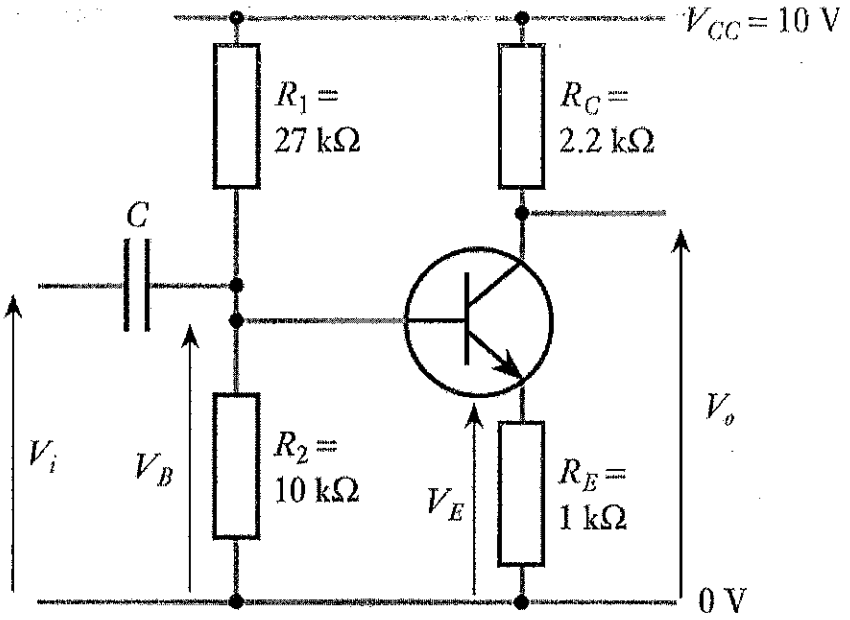


Figure Q4-a

(b) The dc current gain of the transistor of the circuit shown in Figure Q4-b is 200. Determine Q point and draw the dc load line. [08 marks]

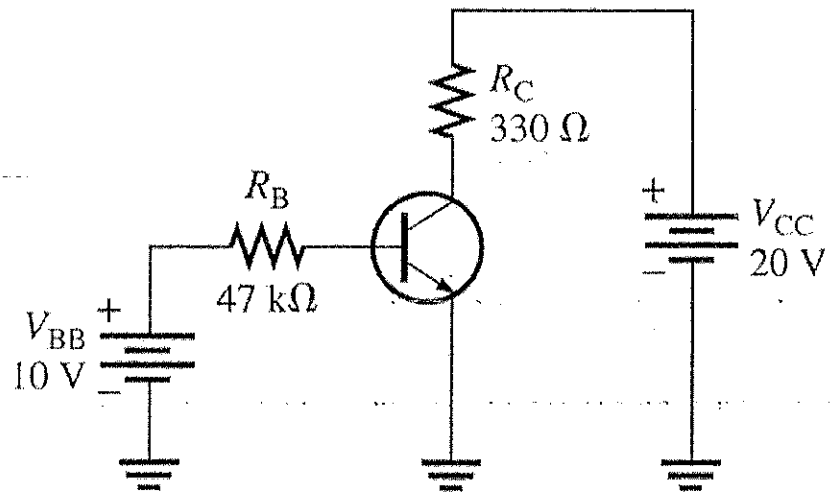


Figure Q4-b

Q5.

(a) List any three characteristics of an ideal operational amplifier and compare with characteristics of real operational amplifier. [06 marks]

(b) Determine the output voltage(Vout) of the operational amplifier circuit shown in Figure Q5-b [06 marks]

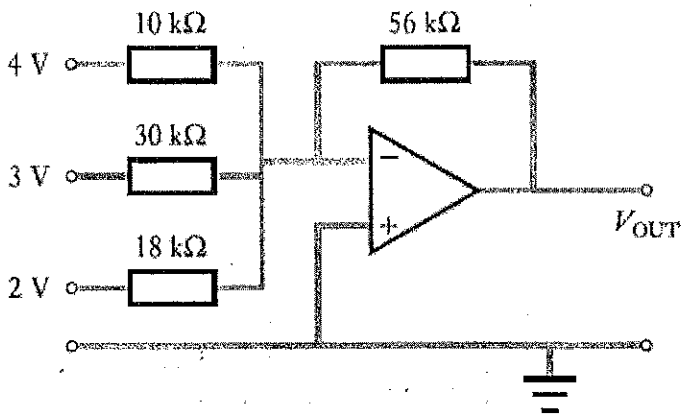


Figure Q5-b

(c)

i. Draw the circuit diagram of an inverting amplifier which uses an operational amplifier. Derive the voltage gain. State any assumptions.

ii. What will be the output voltage of the inverting amplifier, if input voltage 500mV, feedback resistor 10kΩ and input resistor 500Ω.

[08 marks]

Q6.

(a) Perform the following conversions between number systems with clearly showing the necessary steps.

i) 12.4_8 to decimal, binary and hexa-decimal

ii) $5D.2_{16}$ to decimal, binary and octal

[06 marks]

(b) Determine following (8 bit) representations of the -100_{10}. [03 marks]

i) sign magnitude

ii) one's complement

iii) two's complement

(c) Two's complement representation of an 8 bit binary number is given as 11110001. Determine the decimal value of the number. [02 marks]

(d) Design a circuit using logic gates to perform addition of two bit binary numbers. Briefly explain the operation of the circuit using a suitable example. [09 marks]

Q7.

(a) i) Simplify the following Boolean function using K-maps.

$$f(A, B, C, D) = \Sigma m\ (1, 2, 3, 5, 6, 7, 8)$$

ii) Draw the logic circuit using minimum number of gates.

[08 marks]

(b) Determine

i. the minimal sum of product (SOP) and

ii. minimal product of sums (POS)

of the following Boolean expression using k-maps.

$$Q = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BCD + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + A\bar{B}CD$$

[08 marks]

(c) Briefly explain the operation of the shift register using a suitable example.

[04 marks]

Q8.

(a) Complete the corresponding timing diagram of the circuit shown in figure Q8-a.

[08 marks]

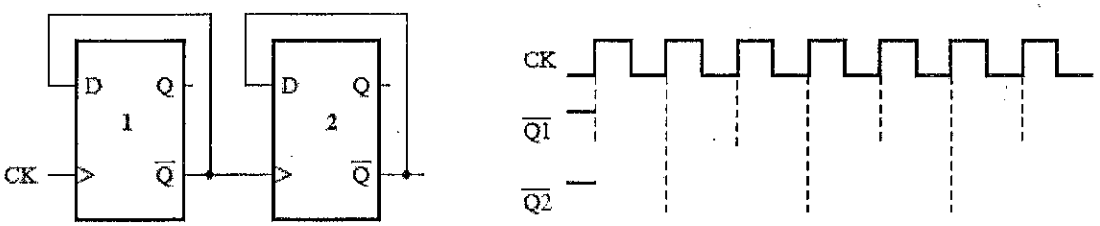


Figure Q8-a

(b) Design a MOD-8 counter using JK flip-flops and logic gates to count in the following sequence: 0, 1, 2, 3, 4, 5, 6, and 7. Show the state transition diagram, present state-next state table, K-map, logic expressions and the circuit implementation clearly.

[12 marks]

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